IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of   :   Customer Number: 20277

                                                :

Shigeki OHBAYASHI   :   Confirmation Number: 8290

                                                :

Application No.: 09/829,046   :   Group Art Unit: 2818

                                                :   Allowed: November 05, 2004

Filed: April 10, 2001   :   Examiner: MAI, Son Luu

                                                :

For: STATIC SEMICONDUCTOR MEMORY DEVICE HAVING T-TYPE BIT LINE
    STRUCTURE

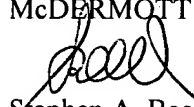## RESPOND TO EXAMINER'S REASONS FOR ALLOWANCE

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The November 5, 2004 Notice of Allowability regarding the above-identified application

included a Statement of Reasons for Allowance. In reviewing the statement we notice a

typographical error. The last line on page 2 reads "11 x N" when it should read "M x N".

Attached is a copy showing the error in red. Please correct the record in this regard.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Stephen A. Becker
Registration No. 26,527

600 13th Street, N.W.   **Please recognize our Customer No. 20277 as**
Washington, DC 20005-3096   **our correspondence address.**
Phone: 202.756.8000 SAB:tlg
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Date: February 3, 2005

DETAILED ACTION

1.   The Petition to Withdraw Holding of Abandonment is granted because the Office

action 11-28-01 was not received by Applicant.

2.   Claims 1-7 are allowed.

3.   The following is an examiner's statement of reasons for allowance: The prior art

of record fails to teach a static semiconductor memory device having T-type bit line

structure using horizontal memory cells to reduce layout area and increase operating

speed.   The static semiconductor memory device comprises: a number M x N (M:

integer not less than 2; N: integer not less than 2) of memory blocks each of which

include a number 8 x M of horizontal memory cells arranged in eight rows by M columns

and which are arrange in M rows by N columns, a word line provided corresponding to

each memory cell row of each memory block, first and second bit lines provided in

common for the number M of memory block rows so as to correspond to each memory

cell column, first and second bit line signal input/output lines provided corresponding to

each memory block and connected to the first and second bit lines of a predetermined

pair of the corresponding M pairs of the first and second bit lines, respectively, first and

second data input/output lines provided corresponding to each memory block row for

inputting/outputting data of the corresponding memory block row, first and second

power supply lines provided corresponding to each memory block row, a global word

line provided corresponding to each memory block row for selecting the corresponding

memory block row, a global column selecting line provided in common for the number

11 x N of memory blocks so as to correspond to each memory cell column for selecting